REMARKS

Overview of the Office Action

Claims 1-8 and 12-15 have been rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 6,100,104 ("Haerle") in view of U.S. Patent Appl. Pub No. 2003/0178626 ("Sugiyama").

Claims 9-11 have been rejected under 35 U.S.C. §103(a) as unpatentable over Haerle in view of Sugiyama, and further in view of U.S. Patent No. 6,110,277 ("Braun").

Status of the claims

Claims 1-15 remain pending

Rejection of claims 1-8 and 12-15 under 35 U.S.C. §103(a)

The Office Action states that the combination of Haerle and Sugiyamai teaches all of Applicants' recited elements. Applicants disagree.

Independent claim 1 recites a method for the production of a plurality of optoelectronic semiconductor chips each having a plurality of structural elements, with each structural element comprising a semiconductor layer sequence, that includes the steps of "forming on the growth surface a mask material layer, with a multiplicity of windows, most of which have an average lateral extent of less than or equal to 1 μm", "essentially simultaneously growing semiconductor layers to form the structural elements on regions of the growth surface that lie within the windows", and "singulating the chip composite base with applied material to form semiconductor chips each having a plurality of the structural elements", which Haerle and Sugiyamai, whether taken alone or in combination, fail to teach or suggest.

Applicants' recited invention is directed to a method for the production of a plurality of optoelectronic semiconductor chips, each having a plurality of structural elements 12 and each structural element comprising a semiconductor layer sequence. Applicants' recited method includes (with reference to the specification) providing a chip composite base 5 having a substrate 4, a semiconductor layer or layer sequence 6, and a growth surface 3, and forming on the growth surface 3 a mask material 11 with a multiplicity of windows 2, most of which have an average lateral extent of less than or equal to 1 μm. The mask material 11 is chosen so that a semiconductor material of the semiconductor layer that is to be grown in a later method step essentially cannot grow on the mask material or can only grow on the mask material in a substantially worse manner than on the growth surface 3. Applicants' recited method further includes essentially simultaneously growing semiconductor layers 8 to form the structural elements 12 on regions of the growth surface 3 that lie within the windows 2, and singulating the chip composite base 5 with applied material to form a plurality of semiconductor chips that each have a plurality of structural elements where each of the structural elements includes a semiconductor layer sequence (see Fig. 2 of Applicants' specification).

The semiconductor layer sequence 6 arranged on the substrate 4 can have an active zone that emits electromagnetic radiation when a voltage is applied (see paragraph [0051] of Applicants' specification).

Haerle discloses a method for fabricating a plurality of LED semiconductor bodies. According to the method of Haerle, the plurality of LEDs are produced by first depositing a mask layer on a main surface of a substrate wafer. A plurality of windows are then formed in the mask layer of Haerle such that the wafer surface is laid bare in the windows. A semiconductor layer sequence that functionally defines the semiconductor bodies is then deposited onto the

main surface in the windows of Haerle. Finally, the wafer of Haerle is divided and severed into individual LEDs (see Figs. 5 and 6 and the Abstract of Haerle).

The Examiner cites Fig. 5 of Haerle and asserts that the semiconductor layer 6 and the substrate 3 together form a layer sequence that is one structural element and that layers 21, 22 and 23 form a layer sequence that is a second structural element. The Examiner also cites Fig. 4 of Haerle as allegedly teaching the step of essentially simultaneously growing semiconductor layers to form the structural elements on regions of the growth surface that lie within the windows. Applicants disagree.

According to Applicants' claim 1, the structural elements are formed within the windows of the mask layer. According to Haerle, the mask layer 4 is formed on the substrate wafer 19, which includes the growth substrate 3 and the semiconductor layer 6 (see Fig. 3 and col. 6, lines 39-42 of Haerle). Therefore, the substrate 3 and the semiconductor layer 6 are arranged under or below the mask layer. In other words, the substrate 3 and the semiconductor layer 6 of Haerle are not grown within the windows of the mask layer. Further, a person skilled in the art would not regard the substrate 3 with the semiconductor layer 6 as a "semiconductor layer sequence" because the substrate 3 of Haerle is not a layer that is grown, as are the layers 21, 22 and 23. Consequently, the substrate 3 with the semiconductor layer 6 of Haerle cannot in any way be considered to be semiconductor layers that form a structural element on a region of the growth surface that lies within the window, as expressly recited in Applicants' claim 1.

Furthermore, according to Haerle, the semiconductor layers, which are deposited on the substrate surface through the mask windows, functionally form the LEDs (see col. 7, lines 1-5 of Haerle). Nothing in Haerle teaches or suggests that the deposited semiconductor layers form structural elements of the resulting semiconductor bodies, or that each of the resulting chips

includes a plurality of structural elements each comprising a semiconductor layer sequence, as also expressly recited in Applicants' claim 1.

Therefore, Haerle fails to teach or suggest a method for the production of a plurality of optoelectronic semiconductor chips each having a plurality of structural elements, with each structural element comprising a semiconductor layer sequence, that includes the step of "essentially simultaneously growing semiconductor layers to form the structural elements on regions of the growth surface that lie within the windows", as recited in Applicants' independent claim 1.

The Examiner also cites col. 7, lines 33-36 and Figs. 5-6 of Haerle as allegedly teaching singulating the chip composite base with applied material to form semiconductor chips each having a plurality of structural elements.

The cited passages and figures of Haerle in fact teach, instead, that once the chip is singulated, each resulting device comprises a semiconductor sequence forming a single LED without any structural elements. This teaching is in stark contrast to Applicants' recited method in which chip singulation of the composite base with applied material results in the formation of a plurality of semiconductor chips, each of which includes a plurality of structural elements each comprising a semiconductor layer sequence.

Furthermore, as is well known to those skilled in the art, the lateral dimensions of optoelectronic semiconductor chips are typically on the order of several hundred μm, with smaller chips having a length of approximately 250 μm, and larger chips having a length of approximately 1000 μm. There is nothing in Haerle that states or suggests that its optoelectronic chips are anything other than standard-sized. Therefore, it follows that the semiconductor layer sequence of each chip taught by Haerle must be in the general range of about 250 to 1000 μm in

its lateral dimensions. Consequently, the semiconductor layer sequence taught by Haerle is wholly unrelated and non-analogous to the plurality of structural elements recited in Applicants' claims, which result in chips on the order of 1 μm or less in lateral dimension. The lateral dimensions of Applicants' recited structural elements are thus more than two magnitudes smaller than the lateral dimensions of the semiconductor layer sequence taught by Haerle, since Applicants' structural elements are produced by selective growth within a very small window having an average lateral extent of less than or equal to 1 μm, as discussed above.

Therefore, Haerle fails to teach or suggest Applicants' recited step of "singulating the chip composite base with applied material to form semiconductor chips each having a plurality of the structural elements".

On page 4 of the Office Action, the Examiner cites case law which states that "where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and the device having the claimed relative dimension would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device", and asserts that Applicants' claim 1 is obvious in view of Haerle and the cited case law. Applicants' disagree.

Firstly, as discussed in detail above, Haerle fails to teach or suggest certain structural elements and method steps expressly recited in Applicants' independent claim 1. Specifically, Haerle fails to teach or suggest "a plurality of optoelectronic semiconductor chips each having a plurality of structural elements with each structural element comprising a semiconductor layer sequence" and "essentially simultaneously growing semiconductor layers to form the structural elements on regions of the growth surface that lie within the windows; and singulating the chip composite base with applied material to form semiconductor chips each having a plurality of the

structural elements", as recited in Applicants' claim 1. Thus, there exist essential differences between Haerle and Applicants' recited invention beyond Applicants' recited window dimensions.

Secondly, Applicants' recited invention does in fact perform differently than the device of Haerle. Specifically, the purpose of Applicants' invention is to provide improved coupling-out of the electromagnetic radiation generated in the chip composite base (see paragraph [0015] of Applicants' specification). In this regard, Applicants' recited window dimensions are chosen to achieve this purpose.

In contrast, Haerle is concerned with a method for fabricating a plurality of light-emitting diode chips and a method for fabricating a plurality of edge-emitting semiconductor laser chips. The object of Haerle is to provide a method of fabricating a plurality of semiconductor bodies which overcomes problems caused by structuring of the Ga(In,Al)N layer sequences on the wafer and disparate thermal expansion coefficients of the available substrate materials such as defects in the semiconductor structures, primarily cracks, holes, etc., which have a lasting adverse effect on the component properties such as ESD stability, service life, etc., and which enables a plurality of semiconductor bodies with precisely defined side surfaces and/or reduced crystal defects to be fabricated in a simple manner, even where semiconductor materials are used that are highly stable in mechanical and chemical terms and/or substrate and epitaxial layer materials are used with lattice constants that differ greatly from one another (see col. 2, lines 24-38 of Haerle).

Typical LED chips have a size of about 0.5 mm x 0.5 mm or more (i.e., the area of a standard LED chip is upwards of about 500 x 500 = 25000 times greater than a chip with a dimension of only 1 μm x 1 μm or less). An LED chip with a size of only 1 μm x 1 μm would

have an extremely low, barely perceivable illumination brightness. Therefore, one skilled in the art would have no reason to create such an LED chip, and hence one skilled in the art would have no motivation to modify the chip of Haerle to a size of only 1 μm x 1 μm, as such a small chip would not provide a useful light-emitting diode chip or edge-emitting semiconductor laser chip.

Alternatively, the Examiner concedes that Haerle fails to teach or suggest forming on the growth surface a mask material layer with a multiplicity of windows, most of which have an average extent of less than or equal to 1 μm. However, the Examiner cites the abstract of Sugiyama and asserts that Sugiyama teaches a semiconductor light emitting element wherein the width of the base of the light emitting element is within the range of 10 nm - 500 nm. Applicant disagrees.

The cited passages of Sugiyama state that "[t]he light-emitting element is provided with a light-extracting surface which is constituted by a finely recessed/projected surface, 90% of which is constructed such that the height of the projected portion thereof having a cone-like configuration is 100 nm or more, and the width of the base of the projected portion is within the range of 10-500 nm".

The cited passages of Sugiyama thus clearly indicate that the disclosed width of 10 nm – 500 nm is simply the width of the base of a recessed/projected portion 18, which is formed on the current diffusion layer 15 (see Fig. 2A, and paragraphs [0035] and [0036] of Sugiyama).

Clearly, the windows of the mask layer described by Sugiyama are not used for growing semiconductor layers, which is in contrast to the recitation of Applicants' claim 1. Sugiyama discloses applying the mask layer on the current diffusion layer 15, and performing an RIE (reactive ion etching) process to transcribe the pattern of the mask layer into the current diffusion layer 15 (see paragraph [0043] and Figs. 3C and 3D of Sugiyama). Sugiyama, therefore, merely

describes a method for producing a surface structure on an already existing semiconductor layer.

Consequently, the width disclosed by Sugiyama of 10 nm - 500 nm is not the width of the base of the light emitting element, as proffered by the Examiner, and therefore has nothing to do with forming on a growth surface of a chip composite base a mask material layer with a multiplicity of windows, most of which have an average lateral extent of less than or equal to 1 μm, as recited in Applicants' claim 1.

Sugiyama thus fails to teach or suggest forming on the growth surface of a chip composite base a mask material layer with a multiplicity of windows, most of which have an average lateral extent of less than or equal to 1 μm, as recited in Applicants' claim 1.

The Examiner further asserts that given the teaching of Sugiyama, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Haerle by employing the well known or conventional feature of windows with an average extent of less than 1 μm in order to produce a light-emitting element with the desired size. Applicants disagree and submit that there is no such motivation to combine the teachings of Haerle and Sugiyama as proffered by the Examiner.

Haerle describes a method for producing a plurality of LED chips on a semiconductor wafer, wherein each chip is grown in the window of a mask layer (i.e. the windows in the mask layer approximate the size of the LED chips).

Sugiyama, on the other hand, describes a method for making a light scattering structure on the surface of an individual LED chip. The purpose of the small surface structures 18 on the top of the chip of Sugiyama is to provide improved light extraction due to surface scattering at the projected portions, which have a size on the order of the wavelength of visible light.

There is simply no reason that one skilled in the art would, on the basis of Sugiyama,

look to reduce the width of the mask windows of Haerle to a size of 1 μm or less, absent Applicants' express teachings, because such a reduced size window would result in individual chips each having a lateral dimension of only 1 μm x 1 μm or less.

As mentioned above, typical LED chips have a size of about 0.5 mm x 0.5 mm or more (i.e., the area of a standard LED chip is upwards of about 500 x 500 = 25000 times greater than a chip with a dimension of only 1 μm x 1 μm or less). An LED chip with a size of only 1 μm x 1 μm would have an extremely low, barely perceivable illumination brightness, and the person of skill would not therefore have any reason to so modify Haerle to create such tiny LED chips. Thus, there would be no technical advantage for one skilled in the art to employ the window size used to form the projected portions of Sugiyama for fabricating the chips of Haerle.

Consequently, Haerle and Sugiyamai, whether taken alone or in combination, fail to teach or suggest each of the steps recited in Applicants' amended independent claim 1.

Independent claim 14 recites limitations similar to those of claim 1 and is, therefore, deemed to be patentably distinct over Haerle and Sugiyamai for at least those reasons discussed above with respect to claim 1.

In view of the foregoing, Applicants submit that Haerle and Sugiyamai, whether taken alone or in combination, fail to teach or suggest the subject matter recited in independent claims 1 and 14. Accordingly, claims 1 and 14 are deemed to be patentable over the combination of Haerle and Sugiyamai under 35 U.S.C. §103(a).

Claims 2-8, 12-13, and 15, which depend from independent claim 1, incorporate all of the limitations of independent claim 1 and are, therefore, deemed to be patentably distinct over Haerle and Sugiyamai for at least those reasons discussed above with respect to claim 1.

Rejection of claims 9-11 under 35 U.S.C. §103(a)

The Office Action states that the combination of Haerle, Sugiyamai, and Braun teaches all of Applicants' recited steps in these claims.

Haerle and Sugiyama have been previously discussed and fail to teach or suggest the subject matter recited in Applicants' independent claim 1.

Because Haerle and Sugiyamai fail to teach or suggest the subject matter recited in Applicants' independent claim 1, and because Braun fails to teach or suggest the subject matter of independent claim 1 that Haerle and Sugiyamai are missing, the addition of Braun to the reference combination fails to remedy the above-described deficiencies of Haerle and Sugiyamai.

Claims 9-11, which depend from independent claim 1, incorporate all of the limitations of independent claim 1 and are, therefore, deemed to be patentably distinct over Haerle, Sugiyamai and Braun for at least those reasons discussed above with respect to independent claim 1.

Conclusion

In view of the foregoing, reconsideration, withdrawal of all rejections, and allowance of all pending claims is respectfully solicited.

Should the Examiner have any comments, questions, suggestions, or objections, the Examiner is respectfully requested to telephone the undersigned in order to facilitate a resolution of any outstanding issues.

It is believed that no fees or charges are currently due. However, if any fees or charges are required at this time in connection with the application, they may be charged to our Patent and Trademark Office Deposit Account No. 03-2412

Respectfully submitted,
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